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PERFORMANCE ASSESSMENT OF III-V HETEROJUNCTION FINFETS AT 14nm GATE LENGTH

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ABSTRACT

Fin shaped field effect transistors have become prominent candidate in high-performance processors of leading semiconductor industries. It is owing to the fact that thin fin of structure and presence of gates on multiple sides increase electrostatic integrity. Objective of the present work is to design FinFET for gate length of 14nm and analyse performance parameters for different channel materials. Fin width and fin height of device is set as 7nm and 12nm; 25nm and 30nm respectively. Channel of FinFET has been structured with III-V type materials such as AlGaAs, InGaAs and InP. Cogenda Visual TCAD tool has been used for accurate design and extensive simulations of FinFET. Performance has been investigated in terms of on-current (Ion), leakage current (Ioff) and subthreshold swing (SS) for applied drain voltage and gate voltage. These parameters have been extracted from current-voltage characteristics of the device. Ion/Ioff is of the order 107, Ioff is of the order 10-14 and SS is around 80mV/dec for InP material. Based on performance comparison, it is noted that superior performance is achieved in case of InP material as compared to other materials.

Keywords: FinFET, heterojunction, Subthreshold swing, fin height, fin width, TCAD.

INTRODUCTION

Heterojunction (HJ) transistors have widely been used for improving the mobility, hence transconductance of device. Materials with heterojunction properties have different band gap and lattice constant (Das 2016). Most of the compound semiconductor materials such as III-V type are used for making non-homogeneous contacts (Dharmarasu 2017).

Transistors with heterojunction channel have a variety of applications in optical devices, high electron mobility devices etc. (Faber 2017). MOSFETs with different channel materials have been explored in literature. However, there are few limitations which made single gate transistors unviable with the shrink in technology node. Thereafter, MOSFETs with aligned gates on upper and lower side of channel were used in devices. Soon tri-gate FinFETs came into existence where polysilicon gate was placed across three sides of channel which ultimately enhanced electrostatic control of gate over channel. Furthermore, short channel effects are under control when multiple gates are kept in the vicinity of electrical channel (Colinge 2008). Multigate Field Effect Transistors have become an integral component of most of the latest processors and smartphone devices.

Sustaining device performance as technology node shrinks down, is a challenging process because Silicon material, a traditional element has its own limits and band gap properties. SiO_2 widely used as gate oxide, cannot control gate tunneling leakage currents if silicon is scaled down to 1 nm. Due to this fact, gate oxide stack concept comes into play where high-k dielectrics such as Al_2O_3, Si_3N_4, HfO_2, ZrO_2 etc. are used a stack with low-k SiO_2 material (Robertson 2004). Apart from this, instead of elemental semiconductors such as Si and Ge, compound semiconductors are being used for channel formation. Si_xGe_{1-x} as channel has mixed properties of Si and Ge which results in enhanced performance (Aujla 2022). Moreover, III-V type compound semiconductors like GaAs, InGaAs, InP, GaP contribute significantly towards device properties and behavior (Hur 2016, Im 2023, Lu 2022, Reddy 2023).

This work throws light on 14nm heterojunction FinFET design by using channel of compound materials InGaAs/GaAs, AlGaAs/GaAs and InP. Further, TCAD simulation setup has been used for simulation and performance comparison of transistor structures for different fin width and fin height.

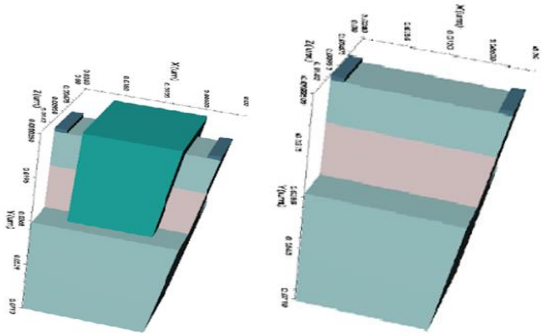
Section 2 describes device dimensions and three-dimensional structures formed in TCAD. Section 3 shows the voltage-current characteristics of designed device for all cases. Section 4 concludes the work and presents future extension of work.

DEVICE DESIGN

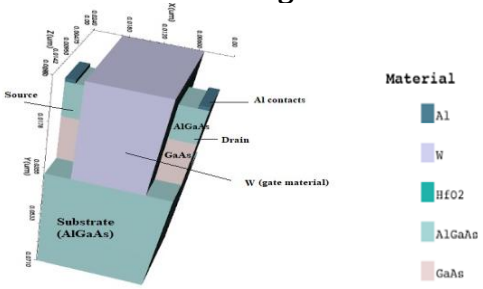
The hetero-junction FinFET structures have been designed with III-V type channel materials such as AlGaAs, InGaAs and InP at 14nm gate length. The device dimensions as shown in Table I have been selected according to the ITRS roadmap specifications. The 3D device structures have been designed and simulated in Visual TCAD environment (Yanfu 2016). The different materials used in different regions of hetero-junction FinFET structures are shown in Fig. 1, Fig. 2 and Fig. 3.

TABLE I. DEVICE DIMENSIONS OF HETERO-JUNCTION FINFET STRUCTURES

Parameters	Dimensions
Length of gate	14 nm
Length of gate oxide	14 nm
Substrate's thickness	30 nm
Length of Source/Drain	10 nm
Fin Height	25nm and 30nm
Fin Width	7nm and 12nm



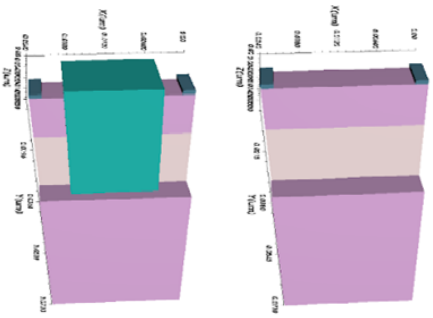
(a) HfO_2 oxide material(b) AlGaAs & GaAs as Active fin region



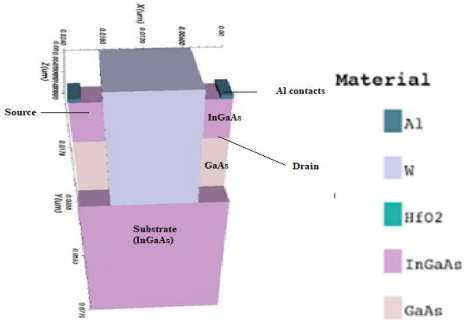
(c) Side view

Fig. 1: Hetero-junction Device 1 FinFET structure for height 25nm and Width 7nm

Device 1 has substrate of Aluminium Gallium Arsenide (AlGaAs) material, whereas active fin and source/drain are of AlGaAs and GaAs. Device 2 has Indium Gallium Arsenide (InGaAs) as substrate; Source, drain and fin are made up of InGaAs and GaAs. Device 3 shows Silicon material for substrate and Indium Phosphide (InP) for fin region. Gate is made up of Tungsten material due to its suitable work function and Hafnium Oxide (HfO_2) is for gate oxide.

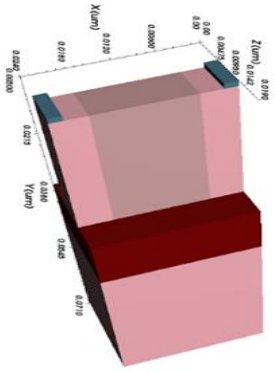


(a) HfO_2 oxide material(b) InGaAs & GaAs as Active fin region

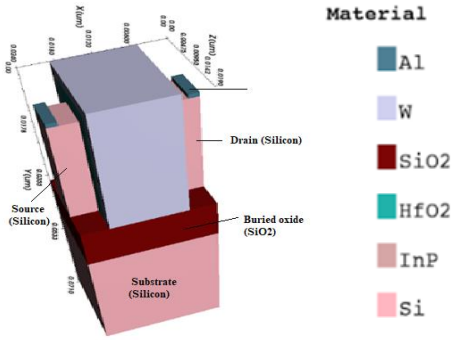


(c) Side view

Fig. 2: Hetero-junction Device 2 FinFET structure for height 25nm and Width 7nm



(a) InP as Active fin region



(b) Side view

Fig. 3: Hetero-junction Device 3 FinFET structure for height 25nm and Width 7nm

RESULTS AND DISCUSSION

The device performance has been assessed in terms of (i) On-current (I_{on}), (ii) off-current (I_{off}), (iii) current ratio (I_{on}/I_{off}) and (iv) Subthreshold Swing (SS) for the designed Heterojunction FinFET structures where properties of III-V type semiconductors have been exploited. TCAD 3D tool has been used for measuring the performance parameters where at 300K temperature, device was simulated for drain voltage of 0.05V and no gate supply to obtain leakage current, and for 1V gate supply, drive-current was noted down. Current ratio is derived by dividing on-current with off-current (leakage). The subthreshold swing is calculated at 50mV drain voltage using following expression:

$$SS = dV_g / d\log(I_d) \qquad (1)$$

Figures 4-6 below demonstrate V_g-I_d characteristics on linear scale for the proposed Device 1, Device 2, and Device 3 FinFET structures for H_{fin} of 25nm and W_{fin} of 7nm. Table II shows simulation results of device 1 FinFET structure for heights 25nm, 30nm and widths 7nm, 12nm. It has been observed that with the increase in height the on-current enhances and SS deteriorates. With the increase in width and height of device off-current also increase and hence SS

deteriorates. Table III shows simulation results of device 2 FinFET structure for heights 25nm, 30nm and widths 7nm, 12nm. Table IV shows simulation results of device 3 FinFET structure for heights 25nm, 30nm and widths 7nm, 12nm. The device 3 demonstrates better SS as compared to device 1 and device 2.

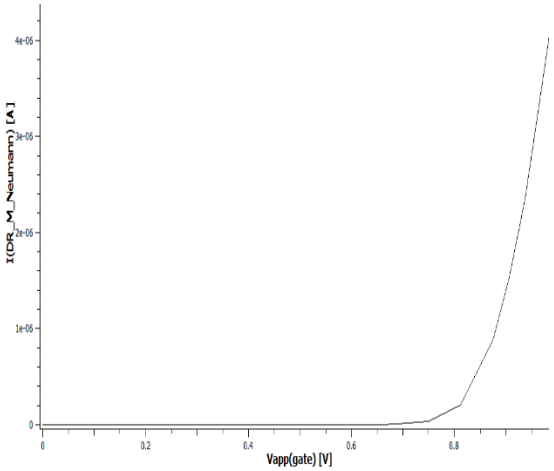


Fig. 4 Transfer characteristics in linear scale for Heterojunction Device 1 FinFET structure at height 25nm and width 7nm.

TABLE II. SIMULATIONS RESULT OF DEVICE 1 FINFET FOR HEIGHTS =25NM , 30NM AND WIDTHS= 7NM, 12NM

Parameter	AlGaAs FinFET (H=25nm W= 7nm)	AlGaAs FinFET (H=25nm W= 12nm)	AlGaAs FinFET (H=30nm W= 7nm)	AlGaAs FinFET (H=30nm W= 12nm)
On-Current, Ion(A)	4.60×10^{-06}	4.43×10^{-06}	4.6152×10^{-06}	2.5×10^{-05}
Off-Current, Ioff(A)	3.03×10^{-12}	3.87×10^{-10}	3.4803×10^{-12}	3.61×10^{-10}
Current ratio, Ion/Ioff	1.51×10^{6}	1.14×10^{4}	1.3260×10^{6}	6.94×10^{4}
SS (mV/dec)	87.3	88.5	96	88.3

TABLE III. SIMULATIONS RESULT OF DEVICE 2 FINFET FOR HEIGHTS =25NM , 30NM AND WIDTHS= 7NM, 12NM

Parameter	InGaAs FinFET (H=25nm W= 7nm)	InGaAs FinFET (H=25nm W= 12nm)	InGaAs FinFET (H=30nm W= 7nm)	InGaAs FinFET (H=30nm W= 12nm)
On-Current, Ion(A)	1.45×10^{-05}	6.55×10^{-06}	1.4644×10^{-05}	1.42×10^{-05}
Off-Current, Ioff(A)	3.22×10^{-10}	8.44×10^{-09}	2.9094×10^{-10}	7.10×10^{-09}
Current ratio, Ion/Ioff	4.50×10^{4}	7.76×10^{2}	5.0333×10^{4}	2.00×10^{2}
SS (mV/dec)	99.8	111.3	99	111

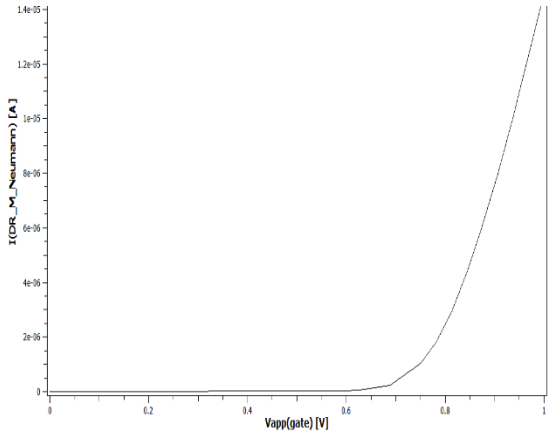


Fig. 5 Transfer characteristics in linear scale for designed Heterojunction Device 2 FinFET structure with height 25nm and width 7nm.

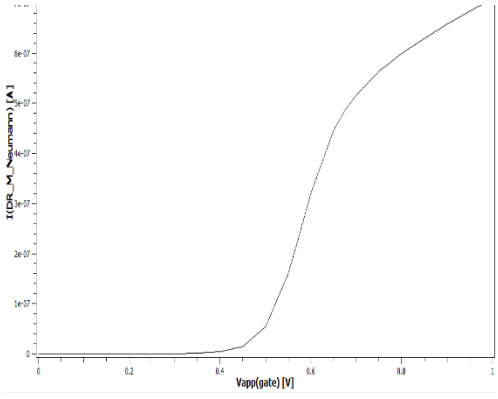


Fig. 6 Transfer characteristics in linear scale for designed Heterojunction Device 3 FinFET structure with height 25nm and width 7nm

TABLE IV. SIMULATIONS RESULT OF DEVICE 3 FINFET FOR HEIGHTS =25NM , 30NM AND WIDTHS= 7NM, 12NM

Parameter	InP FinFET (H=25nmW= 7nm)	InP FinFET (H=25nm W= 12nm)	InP FinFET (H=30nm W= 7nm)	InP FinFET (H=30nm W= 12nm)
On-Current, Ion(A)	7.0845×10^{-07}	8.751×10^{-07}	7.96498×10^{-07}	1.04465×10^{-06}
Off-Current, Ioff(A)	3.3940×10^{-14}	3.7547×10^{-13}	2.84683×10^{-14}	5.48673×10^{-13}
Current ratio, Ion/Ioff	2.08×10^{7}	2.3306×10^{6}	2.7978×10^{7}	1.8225×10^{6}
SS (mV/dec)	79.5	85	80	88

IV. Comparative Analysis of Multigate FinFETs

Table V compares proposed work with existing research. The proposed work shows that leakage current is reduced by factor of 100 (approx.) when compared to work done by Han, 2017 and Kaur et.al, 2020 and this parameter is considerably improved in comparison to simulation results of Lee, 2016. The current ratio of proposed device has shown improvement by 6.5 times, 30 times and 148 times as compared to the reported work in Kaur et al., 2020, Han et al., 2017 and Lee, 2016 respectively. For the similar dimensions of regions such as gate and active fin, the SS is numerically nearly same as SS obtained in Lee, 2016.

Moreover, III-V type FinFET shows improvement in leakage current and current ratio when compared with Silicon based FinFET at the cost of little reduction in on-current.

TABLE V. COMPARATIVE ANALYSIS OF MULTIGATE FINFETS

Parameter	Channel: Indium Phosphide, [Gate length, Fin Height, Fin Width]: [14nm, 25nm, 7nm) (Proposed work)	Channel: Silicon, [Gate length, Fin Height, Fin Width]: [14nm, 45nm, 5nm] (Kaur 2020)	Channel: Silicon, [Gate length, Fin Height, Fin Width]: [20nm, 26nm, 10nm] (Han 2017)	Channel: Silicon, [Gate length, Fin Height, Fin Width]: [14nm, 26nm, 8nm] (Lee 2016)
On-Current, Ion(A)	7.0845×10^{-7}	5.78×10^{-6}	0.35×10^{-6}	14×10^{-5}
Off-Current, Ioff(A)	3.3940×10^{-14}	1.84×10^{-12}	0.5×10^{-12}	1×10^{-9}
Current ratio, Ion/Ioff	2.08×10^{7}	3.14×10^{6}	0.7×10^{6}	0.14×10^{6}
SS (mV/dec)	79.5	62.7	**	77.562.7

** Not calculated in the paper.

V. Conclusion

In this work III-V type semiconductor have been used for FinFET design at 14nm gate length such as AlGaAs, InGaAs and InP. The performance of designed device was measured by extracting parameters such as on-current (Ion), leakage current (Ioff) and subthreshold swing (SS). After extensive simulations in TCAD set-up under gate voltage and drain voltage, it was observed that high value of Ion/Ioff ratio and improved leakage current was obtained for InP channel material. The device designed with InP channel material provides the best results as compared to other channel materials.

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