JOURNAL PUNJAB ACADEMY OF SCIENCES (Peer Reviewed Open Access Journal)
JPAS, 23: 95-100 (January-December, 2023)
Available online at www.jpas.in
ISSN 2229-7014 (P)

SIMULATION METHODOLOGY FOR ANALYZING THE PERFORMANCE OF TFET THROUGH THM-TFET MODEL FILE IN CADENCE

Sri Ch.Pavan Kumar[1] , Gorantala Roshini[2] , Bolloju Pravalika[3], Khansa Simran[4], Nimmakuri Deepthi[5]

Electronics and Communication Engineering, Kakatiya Institute of Technology and Science Warangal Telangana, India[1,2,3,4,5].

chpk.ece@kitsw.ac.in[1], gorantalaroshini06@gmail.com[2] , bollojupravalika@gmail.com[3], khansasimran2512@gmail.com[4] , deepthinimmakuri02@gmail.com[5]

ABSTRACT

MOSFETs are used to create the majority of real-time devices at present due to their fast-switching times. MOSFET subthreshold swing scaling cannot be 60mV/decade lowered. Because of its low subthreshold swing and low leakage current, tunnel FET (TFET) is a viable MOSFET substitute. This paper shows the simulation of the TFET inverter using cadence virtuoso by using the model file called THM-TFET, it is Verilog-A coded and used for the DC and AC simulations of Tunnel FET(TFET).

Keywords: TFET, DG-TFET, THM-TFET

INTRODUCTION

Tunnel FETs are exciting new devices for low-power applications because of their low off-current and the possibility for a tiny subthreshold swing of 60mV/decade (M. Graef et al 2018). Tunnel FETs are gated P-I-N diodes whose current is produced via band-to-band tunnelling. Due to the P-I-N body of the TFET it also eliminates latch-up internally, unlike the MOSFET Double gate tunnel field effect transistor overcomes the limitations of leakage current and sub-threshold slope but it also has a drawback of ambipolarity due to its symmetrical source-drain architecture (F. Horst 2019), the solution for this is to introduce some asymmetry between source and drain this is through the step channel thickness.

As said earlier the model file used here is THM-TFET, which stands for "Thermal-Aware Heterostructure Multi-Gate Tunnel Field Effect Transistor". It is a kind of tunnel field-effect transistor (TFET) designed to outperform conventional TFETs and has greater thermal efficiency. A heterostructure channel and numerous gates are additional design elements found in the THM-TFET that aid to lower device heating and increasing device efficiency. It includes two versions, a charge-based capacitance (AC) model and a DC type. The charge-based capacitance model provides simulation results for AC, transient, and complex analysis, whereas the DC model just provides the I-V properties of the device. This model has been derived to use TFETs as single-gate, double-gate, nanowires TFETs. The structural parameters for these various models are also defined. To match the model to data from measurements or device simulations, it

also includes structural and fitting characteristics of the TFET (TCAD).
The "Compact Solver for Double Gate Tunnel-FETs" tool on nanohub.org likewise uses the model equations of the THM-TFET as coded in Verilog-A, therefore the parameters are also the same and give us the same results for DC and AC characteristics

DC Compact Model

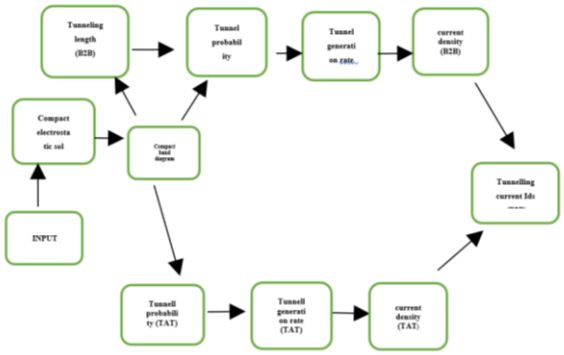

Fig.1: Flow chart of DC modeling

The DC model's structural parameters are defined in this model, which first calculates the 2D potential solution from the data before deriving the electrostatic solution. The band diagram is then explained. The band diagram is used to calculate the tunneling B2B and tunneling TAT. In B2B, the tunnelling probability is calculated using the tunneling length, which is obtained from the band diagram. The rate of tunneling generation and the current density are also calculated. By combining the two findings from B2B and TAT, the total tunnelling current Ids are determined (A. Kloes and T. H. M. NanoP 2021). TAT and ambipolar current have more influence on power and less influence on the speed of the TFET inverter (Farokhnejad, F. Horst, B. Iñíguez, F. Lime, and A. Kloes 2019).

Structural parameters

The structural parameters of the n-type compact DC model are listed below in the table with their values.

TABLE I. DC MODEL PARAMETERS

Parameter	Identifier	Description	Unit	value
Type	TYPE 1	1:n-type, 1:p-type	-	-
l_{ch}	lch	length of the channel	cm	22E-7
l_{sd}	lsd	source/drain length	cm	20E-7
t_{ch}	tch	The thickness of the channel	cm	10E-7
t_{ox}	Tox	The thickness of the oxide		2E-7
w_{ch}	wch	Channel width		1000 E-7
ε_{ox}	esp_r_ox	Gate-oxide permittivity	As/Vcm	22
ε_s	eps_s	Source permittivity	As/Vcm	11.7
ε_d	eps_r_d	Drain permittivity	As/Vcm	11.7
ε_{ch}	eps_r_ch	Channel permittivity	As/Vcm	11.7
N_s	N_s	Source doping concentration	cm-3	1E20
N_d	N_d	Drain doping concentration	cm-3	1E20
N_{ch}	N_ch	Channel doping concentration	cm-3	1E11
E^s_g	Eg_s	Source bandgap	eV	1.12
E^d_g	Eg_d	Drain bandgap	eV	1.12
E^{ch}_g	Eg_ch	channel bandgap	eV	1.08
E_s	E_s	Source degeneration region	eV	0.05
E_d	E_d	Drain degeneration region	eV	0.05
χ_s	X_s	Source affinity	eV	4.05
χ_d	X_d	Drain affinity	eV	4.05
χ_{ch}	X_ch	Channel affinity	eV	4.05
N_T	N_T	Trap-density	cm-2	1E10
V_{fb}	Vfb	Flat-bond voltage	V	0.65
T	T	Temperature	K	300
$\Lambda^{s/d}_{fit}$	Lambda_ fit_s/d	Screening length on the source and drain fitting factor	-	1.5
$\Lambda^{s/d}_{ln,\ fit}$	Lambda_ 0_log_shift_s/d	Inversion Charge's impact on viable solutions	-	1.5
$m^*_{s/d}$	m_n/p	The effective mass of holes and electrons	-	0.26
$(\eta^{s/d})^2$	Eta2_Jy_on/amb	The factor for fitting tunnelling current along the y-axis.	-	1E-13

$(\sigma^{s/d}_{B2B})^2$	Sigma2_TGR_B2B_on/amb	Fitting factor for variance of B2B rate (σ^2)	-	8E-17
$(\sigma^{s/d}_{TAT})^2$	sigma2_TGR_TAT_on/amb	TAT rate (σ^2) variance fitting factor	-	9E-16
$\kappa^{s/d}_{TAT}$	F_slope_TAT_on/amb	The fitting factor for TAT current slope	-	15
$\tau^{s/d}_{TAT}$	tau_on/amb	Fitting factor to capture TAT current cross section	-	2E-18
$x^{s}_{TAT,\ max}$	xmax_TAT	Determining factor for the maximum TAT rate position	-	4E-7
$V_{ds\ sat}$	Vds_sat_on	V_{ds} limitation	-	10
$A_{Vds,sat}$	A_vds_sat	V_{ds} saturation adjustable parameter	-	5
$V_{gs,sat,offs,on}$	Vgs_sat_offset_on	Limitation of V_{gs} offset (on state)	-	10
$V_{gs,sat,offs,amb}$	Vgs_sat_offset_amb	V_{gs} offset limitation (ambipolar state)	-	10
$A_{Vgs,sat}$	A_vgs_sat	V_{gs} saturation adjustable parameter	-	5
$J_{s,diode}$	J_S_Diode	Pin diode saturation current per gate width	A/cm	1E-29
n_{diode}	n_diode	Pin diode ideality factor	-	1
β	beta	On-current enhancement factor	-	1

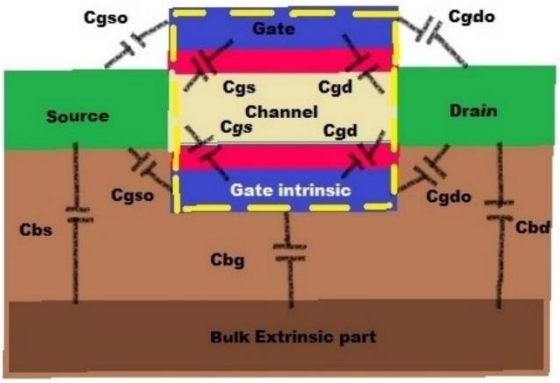

Fig.2: Capacitances in TFET

The accumulation of charge carriers takes place thus capacitive behavior is caused by the TFET structure. There are two types of capacitances: intrinsic and extrinsic capacitances. In the channel region, the intrinsic capacitance is built up and continuously varies in response to the terminal voltages. The intersection of various transistor areas is what causes the extrinsic capacitances. The intersection between the terminals and bulk gives the capacitance CBS, CBD, and CBG.

In a compact model, both intrinsic and extrinsic capacitances must be taken into account. Current and channel charges are the sources of intrinsic capacitance.

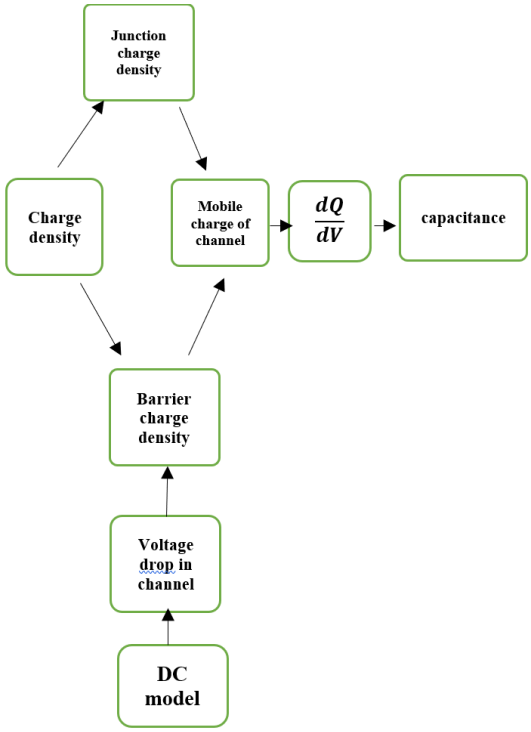

Fig.3: Flow chart of capacitance modeling

The flow chart shows the analytical procedure for the calculation of the total moving charge in the channel.

Due to the voltage drop at the tunnelling barrier from source to channel in the on-state, which takes place at a distance of λb from the source junction, the density of the drain end is practically equal to the moving charge and channel density. The drain contact is directly

responsible for the channel charge that exists between the tunnelling barrier and the source junction.

The drain-to-source voltage drops at the drain-to-channel tunnelling barrier, which is λb distances from the drain junction, when the circuit is ambipolar (A. Farokhnejad, M. Schwarz, F. Horst, B. Iniguez, F. Lime, and A. Kloes 2019). Only the source contact can explain the channel charge that exists between the tunnelling barrier and the source junction. The moving charge in the channel makes the distinction between the on-state and ambipolar state. The n-type TFET's electrons are in the on state, whereas the state of the holes is ambipolar.

PROPOSED AND EXISTING METHODS

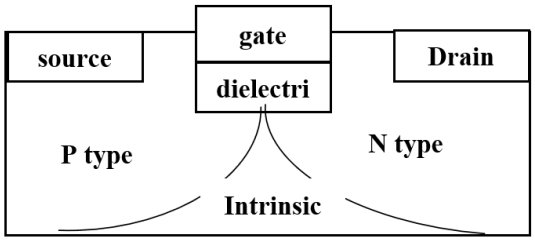

Fig.4: Structure of TFET

The above is the figure of tunnel FET. The tunnel takes place between intrinsic and P+ regions. The energy barriers between the intrinsic and P+ regions are quite wide, measuring roughly 10 nm, and the source terminal is grounded without a gate voltage. The device is turned off. The tunnel barrier gets smaller as Vg rises, making room for current to pass through. The voltage swing is the difference between the threshold voltage and the voltage at which current starts to increase with increasing gate voltage.

The MOSFET has a constant slope between off-state and threshold. A TFET reveals the steeper slope. The voltage swing of a TFET is less than that of a MOSFET. In contrast to MOSFET, the current depends exponentially on the square root of the gate capacitance. In light of this, we focus on device optimization.

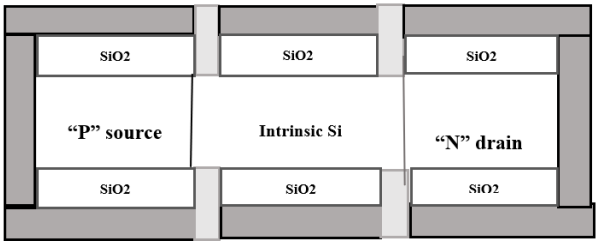

Fig.5: Structure of DG-TFET

By adding another gate, the current through the TFET will increase by double. This enhances on-current while reducing off-current to femto- or pico-ampere levels. The subthreshold swing is also reduced by employing high-k dielectric materials, increasing efficiency (S. Singh and S. S. Chauhan 2017).

RESULTS AND SIMULATIONS

The below figure shows the simulation of the Tunnel-FET(TFET) inverter in cadence virtuoso.

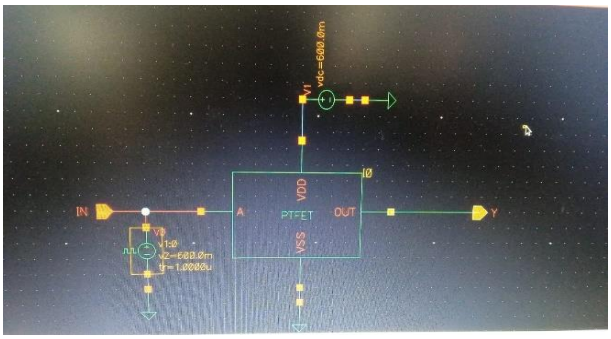

Fig.6: TFET inverter in cadence

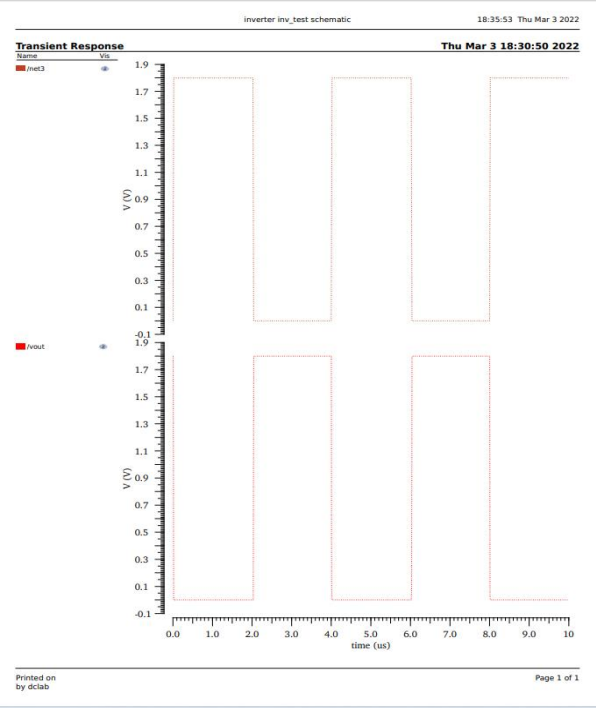

Fig.7: TFET inverter output

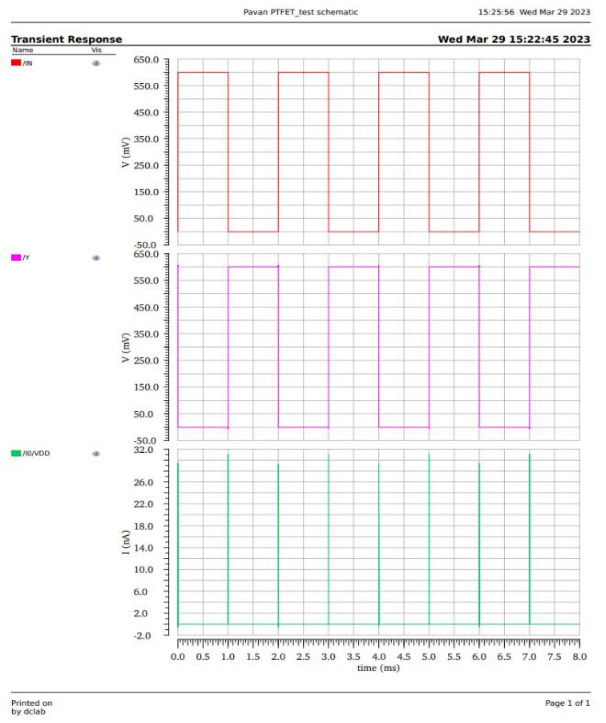

Fig.8: TFET output voltage and output current

The above graph shows the output voltage and current at Vdc equal to 0.6mV. Hence the calculation of average power turned out to be average current is equal to 11.81E-12A, the average voltage is equal to 300E-03V and the average power is equal to 3.54E-12W.

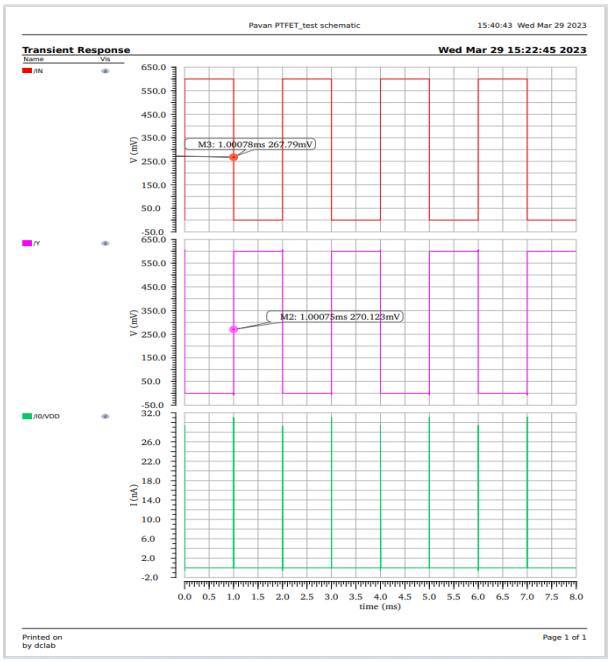

Fig.9: Delay of TFET inverter

The delay of the inverter of its input to the output turned out to be 0.00003ms.

CONCLUSION

In conclusion, the THM-TFET model file used to simulate TFET inverters in Cadence is a promising technology for low-power applications. The THM-TFET model file includes thermal effects that are essential for the precise simulation of TFET devices and offers a complete framework for improving TFET inverter performance. It is feasible to develop TFET inverters with superior performance in terms of power consumption, switching speed, and noise margin by simulating and optimizing various device parameters, such as the doping concentration, gate length, and gate oxide thickness. There is tremendous room for the creation of new applications that utilize the THM-TFET model file to design and optimize circuits that use

TFET inverters, such as amplifiers, filters, and oscillators.

There is a lot of room for the creation of novel TFET inverter-based applications, such as Internet of Things (IoT) gadgets, sensor networks, and medical implants. The future potential for TFET inverters in Cadence utilizing the THM-TFET model file is bright, and there is a lot of room for more research and development in this field, even though there are still issues with the technology, such as process variation. Overall, the THM-TFET model file in Cadence is a great tool for simulating TFET inverters and offers a promising prospect for the advancement of high-performance, low-power electronics.

REFERENCES

A. Farokhnejad, M. Schwarz, F. Horst, B. Iniguez, F. Lime, and A. Kloes, 'Analytical modeling of capacitances in tunnel-FETs including the effect of Schottky barrier contacts', Solid-State Electronics, vol. 159, pp. 191–196, 2019.

A. Kloes and T. H. M. NanoP, 'THM-TFET: A Physics-Based Verilog-A Compact Model of Tunnel-FETs for DC/AC Exploration of New Circuit Concepts', 2021.

Farokhnejad, F. Horst, B. Iñíguez, F. Lime, and A. Kloes, 'Evaluation of Static/Transient Performance of TFET Inverter Regarding Device Parameters Using a Compact Model', in ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), 2019, pp. 202–205.

F. Horst, A. Farokhnejad, Q.-T. Zhao, B. Iñíguez, and A. Kloes, '2-D Physics-Based Compact DC Modeling of Double-Gate Tunnel-FETs', IEEE Transactions on Electron Devices, vol. 66, no. 1, pp. 132–138.2019.

M. Graef et al., 'Advanced analytical modeling of double-gate Tunnel-FETs--A performance evaluation', Solid-State Electronics, vol. 141, pp. 31–39, 2018.

S. Singh and S. S. Chauhan, 'TCAD simulations of double gate tunnel field effect transistor with spacer drain overlap base on vertical Tunneling', in 2017 International conference of Electronics, Communication and Aerospace Technology (ICECA), 2017, vol. 2, pp. 1–4.