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MODELLING AND ANALYSIS OF FULLY INTEGRATED 3:2 SWITCHED CAPACITOR DC-DC CONVERTER

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ABSTRACT

A type of DC-DC power converter known as a switched-capacitor converter efficiently changes one voltage level to another by employing switches and capacitors. They provide high-performance point-of-load voltage regulation for digital systems. This paper investigates general steady-state performance model of 3:2 series-parallel switched capacitor DC-DC converter. The existing basic SC converter analysis is extended to derive minimum achievable power loss for efficiency enhancement that suffers from both conduction and switching losses. The method relies on charge-multiplier approach and analysis is done to achieve 48mA load current realized on a 22 nm technology node. According to the findings, a unit cell's switch size equates to 1Ω on-resistance, and a switching frequency of at least 200 MHz is needed to achieve the target efficiency of more than 85% and an output voltage more than 0.72V.

Keywords: Switched-capacitor converter, charge-multiplier, series-parallel, performance analysis, DC-DC converter.

INTRODUCTION

In modern electronic products, Switched-capacitor (SC) converter is a preferred choice for power conversion due to various advantages like reduced size, high efficiency, light-weight and high power density (Lu, S. 2019). It comprises of a network of switches and capacitors used for energy storage and transfer from input port to the load. On-off switches coupled to flying capacitors are used to charge and discharge capacitors. These capacitors are also called charge-pump converters as charges either delivered to or removed from the load. SC converters, consists of switch capacitor array instead of bulky and noisy magnetic components (inductors), making them suitable for integrated circuit (IC) implementation and space constrained applications. The reduced module size for fully integrated application requires on-chip integration of passive components and power management unit into a single sensor chip (Wu, Y. -E. 2021). Such modules are available in small packages with minimal external components operating with extremely low quiescent current and are the main power supply solution for handheld portable instrumentations (Wu, G. 2015). High power density and suitability for small-scale integration results in widespread use of SC converters. Conversely, the SC converters experience losses predominantly due to capacitors and switches. These losses are modelled and resolved by evaluating steady-state performance of converter and through calculating its output impedances for low and high frequency regions of operation. The impedances in low frequency and high frequency regions are called slow switching limit (SSL) impedance and fast switching limit impedance (FSL) respectively based on charge

multiplier vectors. The dominant losses for FSL and SSL impedances are switch conductive losses and capacitive losses respectively. Overall steady state performance is evaluated based upon total output impedance calculation (Makowski, M. S. 1995).

The work presents in this paper investigates general steady-state performance models built on existing analysis of SC converters. The model is extended to derive minimum achievable power loss for efficiency enhancement, considering the impact of both conduction loss and switching loss. We explore various methods to optimize and compare different SC DC-DC topologies and valid in both slow and fast switching operation (Bi, H. 2023). Various switching losses such as bottom-plate capacitor loss, switch gate capacitor loss are analyzed to study the effect of these losses on converter's power efficiency. The proposed converter is designed to achieve minimum achievable power loss for efficiency enhancement that suffers from both conduction and switching losses. As illustrated in Fig. 1, the optimal switching frequency and switch size are measured from a specific design perspective in order to maximize the power efficiency.

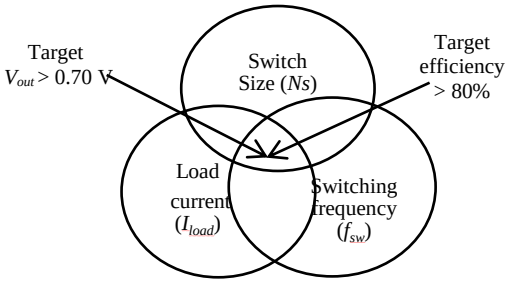


Figure 1: Design parameters of proposed model

The method relies on charge-multiplier approach and analysis is done to achieve load current of 48 mA. The paper is structured as follows, initially a fundamental examination of the proposed 3:2 series-parallel two-phase SC converters based on charge multiplier approach is explained. Further, converter steady-state performance modelling including parasitic is analyzed and the results are discussed.

PROPOSED 3:2 SC DC-DC CONVERTER MODELLING

The 3:2 step down converter, which is depicted in Fig. 2, is used to describe the basic working of SC converters. Each switch in the converter has a 50% duty cycle and operates in two phases: phases 1 and 2. The converter may operate in either common mode or gain mode by changing the switch configuration during each phase. There are total seven switches, two flying capacitors and one load capacitor (single phase). Switches (S_1), (S_3), (S_5), and (S_7) are activated and each flying capacitor is charged from the input voltage during the common mode phase [φ_1]. While in the gain mode phase [φ_2], switches (S_2), (S_4) and (S_6) are on. Each flying capacitor has a direct connection to the output, which allows it to transfer the charge it contains to the load capacitor. Because the output voltage is equal to two-thirds of the input voltage source's value, the gain represents two-thirds of the system's performance.

As converter operates in two region of operation namely SSL and FSL modes of operation. In phase one all those flying capacitor are in series with input supply and charged to input potential (Li, Y. 2022, Stala, R. 2021). In second phase, the capacitors delivering charge to the load known as discharging phase.

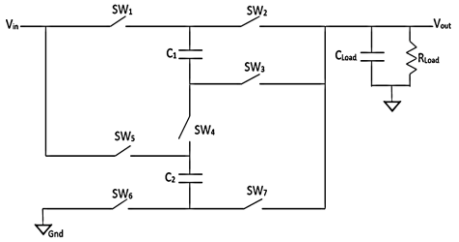
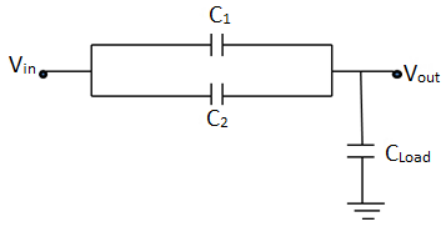
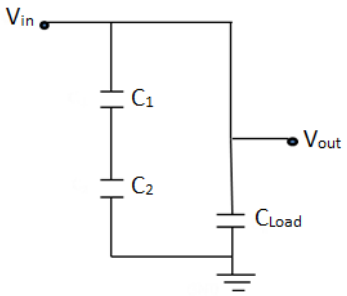


Figure 2: 3:2 series-parallel converter schematic



(a) Phase1



(b) Phase2

Figure 3: 3:2 series-parallel converter configuration in (a) phase1 and (b) phase2 operation.

For calculation of SSL output impedance, the charge multiplier vector for capacitors (a_c) taken single phase due to charge conservation principle) is:

$$a_c = [\ 1/3\ \ 1/3\ \ 1/3\ \ 1/3\ ] \quad (1)$$

We can calculate the average steady-state SSL output impedance as follows:

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_i \frac{(a_{c,i})^2}{c_i f_{sw}} \quad (2)$$

Where $(a_{c,i})^2$ = 4/9 , C_i is the capacitance associated with each capacitor and f_{sw} is the switching frequency of the converter. For two phase 3:2 series-parallel converters, the total R_{SSL} will be half of earlier (which is for single phase).

Fast switching limit (FSL) is a condition when the current flowing across capacitors is almost constant. Voltages in capacitors are modeled as constant. Conduction loss in resistive components is a contributing factor of circuit loss, independent of capacitor voltage-ripple loss. The switch charge-multiplier vector is the single factor that influences the current through the switches (Saadatizadeh, Z. 2020). The output current is used to express the charge flow in the switches (q_r^j):

$$q_r^j = a_r^j q_{out} = a_r^j \frac{I_{out}}{f_{sw}} \quad (3)$$

Where, q^j_r is the switch charge-flow vectors in phase j. Hence, switch charge multiplier vector (a_r) in phase1 is specified as:

$$a_r = [1/3\ \ 1/3\ \ 1/3\ \ 1/3] \quad (4)$$

And in phase2 is given as below:

$$a_r = [1/3\ \ 1/3\ \ 1/3] \quad (5)$$

It is simple to calculate the current in each switch given the charge flow vector. For calculation of fast switching limit output impedance, the charge multiplier vector for switches in both phases (common & gain) is given as:

$$a_r = [\ 1/3\ \ 1/3\ \ 1/3\ \ 1/3\ \ 1/3\ 1/3\ 1/3\ ] \quad (6)$$

The value for this metric is computed as: $(a_r)^2$=7/9 which results in FSL impedance (R_{FSL})as:

$$R_{FSL} = 2\sum_i R_{on,i}\left(a_{r,i}\right)^2 \quad (7)$$

$$R_{FSL} = {}^{14}/_{9}\ R_{on,i} \quad (8)$$

For two phase converter:

$$R_{FSL} = {}^{7}/_{9}\ R_{on,i} \quad (9)$$

where $R_{on,i}$ is the i^{th} switch on-resistance and R_{FSL} is the FSL output impedance and is independent of frequency. Similarly, as defined in case of R_{SSL}, the R_{FSL} value is also reduced to half in case of two phase 3:2 series-parallel converters as resistances (in two phases) are coming in parallel, the total R_{FSL} will be half of earlier (which is for single phase).

PERFORMANCE ANALYSIS WITH PARASITICS

The performance of SC converters is adversely impacted by the numerous parasitic that are connected to MOSFET transistors. The switching of parasitic capacitors causes all the circuit's three main losses involving transistors (Lei, H. 2018). These losses are inversely correlated with switching frequency and switch conductance (or area). The gate capacitance is the main source of parasitic loss (Krstic, M. 2018).

As a straight addition leads in an total impedance greater than anticipated output impedance value, the equivalent output resistance is the quadratic sum of R_{FSL} and R_{FSL}. Hence, the total output impedance is given by

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad (10)$$

The losses relating to SSL and FSL impedances can be used to define the conduction power loss (P_{RES}). Power loss caused by SSL impedance is calculated as:

$$P_{loss,SSL} = I_{out}^2 R_{SSL} \quad (11)$$

where, I_{out} is the output current.

The power loss resulting from FSL impedance is provided by:

$$P_{loss,FSL} = I_{out}^2 R_{FSL} \quad (12)$$

The overall conduction power loss is therefore represented as:

$$P_{RES} = \sqrt{\left(P_{loss,SSL}^2\right) + \left(P_{loss.FSL}^2\right)} \quad (13)$$

Switching loss occurred due to gate capacitance (C_{sw}), bottom plate capacitance (C_{bott}) and equivalent series resistance (ESR) (Peetala, K. 2020). Therefore, total parasitic capacitance and voltage swing at a particular node can be used to estimate total switching power loss (P_{sw}) by summation over all switching nodes of converter given as:

$$P_{sw} = P_{loss,swcap} + P_{loss,bottcap} + P_{loss,esr} \quad (14)$$

The over-all power loss (P_{loss}) the sum of switching and conduction power losses expressed as:

$$P_{loss} = P_{RES} + P_{sw} \quad (15)$$

This novel model works well for simulating and building SC converters that consider parasitic effects. The operating point is chosen to produce the least amount of equivalent resistance while preserving minimal switching losses (Sai, T. 2018). The formula for the output power is

$$P_{out} = \frac{V_{out}^2}{R_{load}} \quad (16)$$

where R_{load} is the load resistance and V_{out} is the optimal output voltage. The network model in Fig. 2 is subjected to voltage division, and the calculated output voltage through the load is shown by

$$V_{out,actual} = V_{out} \frac{R_{load}}{(R_{load}+R_{out})} \quad (17)$$

The efficiency η of the two phase 3:2 series-parallel converter is given by

$$\eta = \frac{P_{out}}{P_{out}+P_{loss}} \quad (18)$$

SIMULATION RESULTS

Input voltage of 1.24 V is considered for modelling of the proposed converter. Load resistance is calculated as 15 Ω equivalent to 48 mA load current for target output voltage of 0.72 V.

Table 1. Inputs to the model

Input parameter	Symbol	Value assigned
Input voltage	V_{in}	1.24V
Ideal ratio	Ratio	2/3
Load resistance	R_L	15 Ω
R_{on} of unit switch cell	R_{on}	50 Ω
Switch parasitic	C_{sw}	10fF
Flying capacitor	C_{fly}	0.4nF
Bottom plate capacitor	C_{bott}	C_{fly}/1000
ESR	R_{esr}	2 ohms

The V_{GS} is equal to 0.9 V and the R_{on} value of 50 corresponds to PMOS/NMOS switch size is evaluated by considering multiples of this basic switch. C_{sw} accounts for total gate capacitor (C_{gs}+C_{gd}), C_{db} for each switch. Each flying capacitor's value is taken as 0.4 nF where C_{bott}

is equal to C_{fly}/constant (constant = 1000) resulting in value of C_{bott} equals to 0.4 Pf as shown in Table 1. It has shown that in order to achieve the target efficiency of more than 80% and the target output voltage of more than 0.70 V, a switch size (R_{on}) of 1 ohm is needed. Findings reveal a maximum efficiency of 86.7% for a target load current of 48 mA at an output voltage of 0.72 V. Number of switches (*Ns*) considered as 50 which results in R_{on} (R_{on} / Ns) equals to 1 Ω.

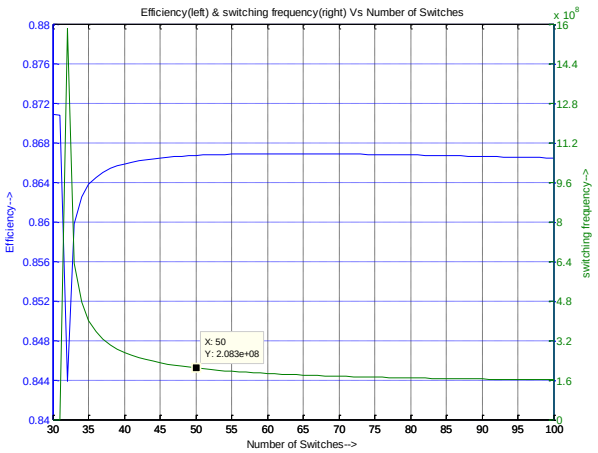


Figure 4. Plot showing efficiency vs N_s (switch size) vs switching frequency for a given Target V_{out} (0.72V) and Target I_{load} (48mA)

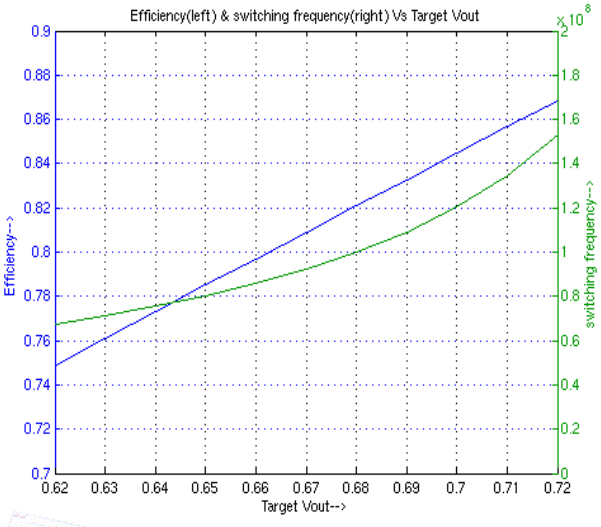


Figure 5. Plot showing efficiency vs V_{out} vs switching frequency for a given switch size (N_s:50) and Target I_{load} (48mA)

Table 2. Results summary

Parameters	Optimum Values
Maximum efficiency	86.7 %
Output voltage (V_{out})	0.72 V
Load current (I_{load})	48 mA
Number of switches (N_s)	1 Ω

Performance trade-offs are evaluated for target V_{out} ranging from 0.62 V to 0.72 V where number of switches (N_s) taken as 50 for target I_{load} of 48 mA and load resistance is calculated as target I_{load} divided by target V_{out} (48 mA/Target V_{out}).

CONCLUSION

For an efficient converter there is a requirement of selecting the best topology for a given application. Meanwhile the technology accounts to device a converter plays a vital role for selecting the finest topology. In SC converters, the power consumption is inversely related to its equivalent output impedance and it is directly related to the square of output voltage for constant output impedance. Two metrics are evaluated, one for the SSL impedance is calculation and another is for the FSL output impedance calculation. These performance metrics relates the converter power to the total V-A based device metrics. The model is extended to derive minimum achievable power loss for efficiency enhancement, that contain both conduction and switching loss. Here we propose a SC DC-DC converter with output current support and efficiency exceeding 80%. Using MATLAB tool, the ideal switch size and switching frequency are

determined in order to maximize efficiency for the given load current and target output voltage. The computation realizes the mathematical framework for efficiency conduction and switching power loss for a converter.

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